

CLAIMS

1. A semiconductor device characterized: in that an elastomer layer is formed over a plurality of 5 semiconductor elements and bonding pads, which are formed over a plurality of chip areas of the principal face of a semiconductor wafer; and in that bump electrodes are electrically connected at their one-end portions with said bonding pads through through holes 10 opened in said elastomer and at their other end portions with wires arranged over said elastomer layer.
2. A chip size package type semiconductor device comprising semiconductor chips obtained by dividing 15 the chip area of said semiconductor wafer as set forth in Claim 1.
3. A semiconductor device as set forth in Claim 2, characterized in that a protective layer is formed on the side faces of said semiconductor chip.
- 20 4. A semiconductor device as set forth in Claim 1, characterized: in that said wires are formed over one face of an insulating tape jointed to the upper face of said elastomer layer; and in that said wires and said bonding pads are electrically connected through 25 Au bumps jointed over said bonding pads.

5. A semiconductor device as set forth in Claim 4, characterized in that a plurality of stages of Au bumps are jointed to the upper faces of said bonding pads.

5 6. A semiconductor device as set forth in Claim 4, characterized in that said Au bumps are sealed with a resin filled in the through holes of said elastomer layer.

10 7. A semiconductor device as set forth in Claim 1, characterized in that said elastomer layer is made of either a photosensitive resist applied to the principal face of said semiconductor wafer or a photosensitive film adhered to the principal face of said semiconductor wafer.

15 8. A semiconductor device as set forth in Claim 1, characterized in that said elastomer layer has a modulus of elasticity of 1 to 5,000 MPa.

9. A semiconductor device as set forth in Claim 1, characterized in that said elastomer layer has a modulus of elasticity of 1 to 1,000 MPa.

20 10. A semiconductor device as set forth in Claim 1, characterized in that said elastomer layer has a modulus of elasticity of about 1 to 500 MPa.

11. A semiconductor device as set forth in Claim 1, 25 characterized in that said elastomer layer has a film

thickness of 0.005 to 0.15 mm.

12. A semiconductor device as set forth in Claim 1,
characterized in that said elastomer layer has a film
thickness of 0.01 to 0.1 mm.

5 13. A semiconductor device as set forth in Claim 1,
characterized in that said elastomer layer has a film
thickness of 0.02 to 0.1 mm.

10 14. A semiconductor device as set forth in Claim 1,
characterized in that said bump electrodes have a
spacing larger than that of said bonding pads.

15. A semiconductor device as set forth in Claim 1,
characterized in that said elastomer layer has an
undulated surface.

15 16. A semiconductor device as set forth in Claim 1,
characterized in that said elastomer layer in the
vicinity of said bump electrodes have slits.

17. A semiconductor device as set forth in Claim 1,
characterized in that the wires arranged over said
elastomer layer are formed at least partially to have
a curved pattern.

18. A semiconductor device as set forth in Claim 1,
characterized in that the wires arranged over said
elastomer layer are formed at least partially to have
a plurality of wires.

25 19. A semiconductor device as set forth in Claim 1,

characterized: in that the wires arranged over said elastomer layer are oriented at a right angle with respect to the direction joining the bump electrodes connected with said wires and the center of said chip area; and in that the wires arranged at the peripheral edge portion of said chip area are longer than the wires arranged at the center portion of said chip area.

20. A process for manufacturing a semiconductor device, comprising:

- (a) forming an elastomer layer over a plurality of semiconductor elements and bonding pads, which are formed in a plurality of chip areas of the principal face of a semiconductor wafer;
- (b) forming through holes over said bonding pads or the electrode wires which are electrically connected with said bonding pads, by opening said elastomer layer;
- (c) forming wires to be electrically connected at their one-end portions with said bonding pads through said through holes and to be arranged at their other end portions over said elastomer layer; and
- (d) connecting bump electrodes with the other end portions of the wires arranged over said elastomer layer.

21. A process for manufacturing a semiconductor device, comprising:

(a) forming an elastomer layer over a plurality of semiconductor elements and bonding pads, which are

5 formed in a plurality of chip areas of the principal face of a semiconductor wafer;

(b) forming through holes over said bonding pads or the electrode wires which are electrically connected with said bonding pads, by opening said elastomer

10 layer;

(c) jointing an insulating tape having wires on its one face to the upper face of said elastomer layer to connect the one-end portions of said wires and said bonding pads electrically through said through holes;

15 and

(d) connecting bump electrodes with the other end portions of the wires arranged over said elastomer layer.

22. A semiconductor device manufacturing process as set forth in Claim 20 or 21, further comprising:

~~dicing and dividing the chip areas of said semiconductor wafer into semiconductor chips.~~

23. A semiconductor device manufacturing process as set forth in Claim 22, further comprising: making a

25 test prior to dicing and dividing said chip areas into

said semiconductor chips, to classify said plurality of chip areas into non-defective and defective ones.

24. A semiconductor device manufacturing process as set forth in Claim 22, further comprising: forming a

5 fuse using at least a portion of the wires arranged over said elastomer layer, to blow the fuse of the chip areas which are determined to be defective by said testing.

25. A semiconductor device manufacturing process as set forth in Claim 20 or 21, further comprising: forming slits in the principal face or back face of said semiconductor wafer at the boundary of said chip areas, and forming protective layers in said slits.

26. A process for manufacturing a semiconductor device, comprising:

(a) forming a plurality of semiconductor elements and a plurality of bonding pads over the individual principal planes of a plurality of chip areas defined by scribe lines;

20 (b) forming an elastomer layer over the principal
faces of said plurality of chip areas;

(c) forming through holes in said elastomer layer at positions, as corresponding to said plurality of

25 areas:

(d) forming such conductive layers individually in
said plurality of chip areas which are formed at their
one-end portions over said elastomer layer and
connected at their other end portions with the
5 corresponding ones of said bonding pads through said
through holes;

(e) forming ~~bump~~ electrodes individually in said
plurality of ~~chip~~ areas which are connected with the
one-end portions of said conductive layers; and

10 (f) cutting said semiconductor wafer along said
scribe lines to form over its principal face a
plurality of semiconductor chips having said elastomer
layers, said conductive layers and said ~~bump~~
electrodes.

15 27. A semiconductor device manufacturing process as
set forth in Claim 26, characterized: in that said
elastomer layer is formed of a photosensitive film;
and in that said through holes are formed by the
photolithography technique and the etching technique.

20 28. A semiconductor device manufacturing process as
set forth in Claim 26, characterized in that the step
(d) of forming said conductive layers includes:
forming Au bump electrodes over said bonding pads; and
forming a wiring layer over said Au bump electrodes.

25 29. A semiconductor device manufacturing process as

set forth in Claim 26, characterized in that the step
(d) of forming said conductive layers includes:
forming a metal layer all over the surface of said
elastomer layer including the insides of said through
holes; and forming a wiring layer by patterning said
metal layer.